Semiconductor Processing Method of Forming Field Effect Transistors", naming Jigish D. Trivedi, Zhongze Wang and Rongsheng Yang as inventors, the disclosure of which is incorporated by reference.

In the Claims

Please cancel claims 1-37 and add claims 38-49 as follows:

CLAIMS

38. (New) Integrated circuitry comprising a semiconductor substrate having an area within which a plurality of n-type and p-type field effect transistors are formed, the respective transistors comprising a gate, a gate dielectric layer and source/drain regions, the gate dielectric layer of the p-type field effect transistors comprising an oxide having nitrogen atoms therein, and the nitrogen atoms being higher in concentration within the gate dielectric layer at only one elevational location as compared to another elevational location, the gate dielectric layer of the n-type field effect transistors being different in composition from the gate dielectric layer of the p-type field effect transistors.

39. (New) The integrated circuitry of claim 38 wherein the gate dielectric layer of the p-type transistors comprises silicon dioxide.

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40. (New) The integrated circuitry of claim 38 wherein the gate dielectric layer of the p-type transistors are of a different thickness relative the gate dielectric layer of the n-type transistors.

41. (New) The integrated circuitry of claim 38 wherein the concentration of nitrogen atoms in the gate dielectric layer of the p-type transistors at the one elevational location is from 0.1% molar to 10.0% molar.

42. (New) The integrated circuitry of claim 38 wherein the one elevational location is located proximate an interface of the gate dielectric layer with the semiconductor substrate.

43. (New) Integrated circuitry comprising a semiconductor substrate having an area within which a plurality of n-type and p-type field effect transistors are formed, the respective transistors comprising a gate, a gate dielectric layer and source/drain regions, the gate dielectric layer of the p-type field effect transistors comprising silicon dioxide having nitrogen atoms therein, the nitrogen atoms being higher in concentration within the gate dielectric layer at only one elevational location as compared to another elevational location and at a concentration of from 0.1% molar to 10.0% molar, the gate dielectric layer of the n-type field effect transistors comprising silicon dioxide material proximate an interface of the gate dielectric layer with the semiconductor substrate which is substantially void of nitrogen atoms.

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44. (New) The integrated circuitry of claim 43 wherein the one elevational location is located proximate an interface of the gate dielectric layer with the semiconductor substrate.

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45. (New) Integrated circuitry comprising a semiconductor substrate substantially devoid of nitrogen atoms and having an area within which a plurality of n-type and p-type field effect transistors are formed, the respective transistors comprising a gate, a gate dielectric layer and source/drain regions, the gate dielectric layer of the p-type field effect transistors comprising an oxide having nitrogen atoms therein, the gate dielectric layer of the n-type field effect transistors being different in composition from the gate dielectric layer of the p-type field effect transistors.

46. (New) The integrated circuitry of claim 45 wherein the nitrogen atoms are higher in concentration within the gate dielectric layer at only one elevational location as compared to another elevational location.

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47. (New) Integrated circuitry comprising a semiconductor substrate substantially devoid of nitrogen atoms and having an area within which a plurality of n-type and p-type field effect transistors are formed, the respective transistors comprising a gate, a gate dielectric layer and source/drain regions, the gate dielectric layer of the p-type field effect transistors comprising silicon dioxide having nitrogen atoms therein, the gate dielectric layer of the n-type field effect transistors comprising silicon dioxide material proximate an interface of the gate dielectric layer with the semiconductor substrate, the silicon dioxide material being substantially void of nitrogen atoms.

48. (New) The integrated circuitry of claim 47 wherein the nitrogen atoms being higher in concentration within the gate dielectric layer at only one elevational location as compared to another elevational location.

49. (New) The integrated circuitry of claim 47 wherein the nitrogen atoms being higher in concentration within the gate dielectric layer at only one elevational location as compared to another elevational location and at a concentration of from 0.1% molar to 10.0% molar.